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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,146	10/29/2003	Michael B. Galles	062986.0296	5506

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EXAMINER	
TREAT, WILLIAM M	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,146	GALLES ET AL.	
	Examiner	Art Unit	
	William M. Treat	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. The examiner is unable to find, in applicants' original disclosure, support for the claim language in claim 1 reciting "a central processing unit having an integrated memory controller operable to control access to the integrated memory nor support for the claim language in claim 16 reciting "a memory controller integrated in the central processing unit and operable to control access to and from local memory". There is nothing supporting the claim to the CPU having such a memory controller though there is support for the processor having such a controller. For this reason the examiner views the quoted language as representing new matter.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-10 and 16-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. As to why the examiner cites claims 1-10 and 16-20 as failing to point out and distinctly claim applicants' invention, see paragraph 4, *supra*.

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-2 and 4-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Kabemoto et al. (Patent No. 5,890,217).

10. The examiner would suggest applicants read col. 16, line 5 through col. 20, line 18 and col. 28, line 55 through col. 29, line 10, at a minimum, before responding.

11. The arguments and rejections presented in the examiner's previous rejections, including those of parent application 09/418,520, continue and are hereby incorporated by reference.

12. Claims 1-2, 5-6, 9-11 and 13-17 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Chase et al. (Patent No. 5,944,780).

13. The examiner would suggest applicants read (col. 5, line 30 through col. 6, line 20; col. 7, lines 44-61; and col. 8, lines 42-48), at a minimum, before responding.

14. The arguments and rejections presented in the examiner's previous rejections, including those of parent application 09/418,520, continue and are hereby incorporated by reference.

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 3, 10, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chase et al. (Patent No. 5,944,780).

18. The arguments and rejections presented in the examiner's previous rejections, including those of parent application 09/418,520 (in relation to claims 10, 18, and 20), continue and are hereby incorporated by reference.

19. As to claim 3, Chase taught the invention of independent claims 1 and 2 from which claim 3 depends (see paragraphs 6-8, *supra*). He did not teach overwriting the

oldest memory reference with a new memory reference upon reaching a buffer limit nor any specific replacement strategy for such a situation. However, the examiner takes Official Notice of the fact that the least-recently-used method of replacement in caches is old, well-known, and one of the conventional methods of cache replacement. In fact, there are at least 267 patents making reference to it as a replacement strategy in subclass 711/133, alone, with the oldest one having been issued a quarter century ago. One of ordinary skill would be motivated to use the least-recently-used replacement strategy with Chase because it is a conventional method which is well-known and well-understood by those of ordinary skill and is, therefore, easily and reliably implemented.

20. Claims 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabemoto et al. (Patent No. 5,890,217).

21. As to claim 3, Kabemoto taught the invention of independent claims 1 and 2 from which claim 3 depends (see paragraphs 6-8, *supra*). He did not teach overwriting the oldest memory reference with a new memory reference upon reaching a buffer limit nor any specific replacement strategy for such a situation. However, the examiner takes Official Notice of the fact that the least-recently-used method of replacement in caches is old, well-known, and one of the conventional methods of cache replacement. In fact, there are at least 267 patents making reference to it as a replacement strategy in subclass 711/133, alone, with the oldest one having been issued a quarter century ago. One of ordinary skill would be motivated to use the least-recently-used replacement strategy with Chase because it is a conventional method which is well-known and well-understood by those of ordinary skill and is, therefore, easily and reliably implemented.

22. The examiner is unable to determine the true scope of applicants' claims 1-10 and 16-20, see paragraphs 2-7, *supra*, so the examiner has merely repeated his earlier rejection of those claims. As to amended claim 11, note that it is merely previously rejected claim 11 with much of the substance of previously rejected claim 13 incorporated therein. The only slight difference which might be perceived between current claim 11 and previously rejected claims 11 and 13 is the statement of the self-evident that when a memory reference is not found in the memory directory for the local memory then the reference is not to local memory but to a remote memory location. None of the amendments to claim 11 constitute patentable differentiation.

23. Applicant's arguments filed 12/8/2005 have been fully considered but they are not persuasive.

24. Applicants' have argued that claims 1-10 and 16-20 are consistent with applicants' original disclosure and are not indefinite, citing Fig. 2 as their explanation. The following are the two points in applicants' specification where Fig. 2 is discussed. On page 6, lines 9-10: "FIG. 2 illustrates a block diagram of a processor within the multi-processor system". On page 8, line 24 through p. 9, line 31: "FIG. 2 is a block diagram of a processor 12. Processor 12 includes memory 16, a memory controller 30, memory directory 18, one or more network interfaces 32, and a CPU controller 34. Network interfaces 32 provide a communication capability between processor 12 and external switch 22. Memory controller 30 controls the read and write access from and to memory 16. CPU controller 34 controls flow between one or more processing units. The size of memory directory 18 may vary according to the size of its associated

memory 16. For example, a processor 12 holding eight megabytes with sixty-four byte lines of cache in a four to one ratio may use 2(17) entries. Using a four gigabyte dynamic random access memory for memory 16, memory references may be represented by thirteen bit tags, two state bits, four pointer/vector bits and two error correction code (ECC) bits. With twenty-one bits per entry and 2(17) entries, memory directory 18 has a size of 2.6 Megabytes. As another example, a processor 12 holding thirty-two megabytes with one hundred twenty-eight byte lines of cache in a four to one ratio may use 2(18) entries. Using an eight gigabyte dynamic random access memory for memory 16, memory references may be represented by twelve bit tags, two state bits, four pointer/vector bits and two ECC bits. With twenty bits per entry and 2(18) entries, memory directory 18 has a size of 5 Megabytes. With the presence of external directory 22, each memory directory 18 may be set up to track its local memory 16 cached memory references. External directory 22 may be set up to track remote cached memory references for the processors 12. Through the use of memory directories 18 and at each processor 12 and external directories 22 in a large multi-processor system 10 environment, cache coherency is provided to ensure that all processors 12 have an accurate view of the entire system memory. Requests for memory may even be passed from one external switch 14 to another to further extend the memory and access mechanism of multi-processor system 10."

25. As best the examiner is able to determine, applicants were describing in Fig. 2 an embodiment of a **processor** within the multiprocessor system as stated throughout their written description of Fig. 2 and that in the embodiment depicted in Fig. 2 the CPU

controller is designated by reference numeral 34. Applicants have identified their CPU controller (34) and their memory controller (30) as separate entities in their drawings. There is nothing in their original disclosure that describes whether the CPU controller (34) box and the memory controller (30) box represent two boards, two chips, etc. The fact that Fig. 2 has a box drawn around the CPU controller (34) box and the memory controller (30) box says nothing about how the two boxes would be constructed. As shown in Figure 2 and as described in applicants' specification, applicants' CPU controller (34) and memory controller (30) do not seem to be integrated except in the sense they work with one another in terms of hardware and software. If applicants are arguing something else for the claim language, this makes the subject matter of claims 1-10 and 16-20 new matter and also renders the scope of these claims indefinite. If they are not arguing anything more than they work with one another in terms of hardware and software, then the previous rejections of applicants' claims still apply.

26. In reference to claim 11 and its dependents, applicants are repeating arguments the examiner dealt with exhaustively in parent application 09/418,520 so the examiner would refer them to that application. However, in response to applicants' argument that "Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor", the examiner would reiterate applicants' original disclosure never offered a definition for integrated. And, while Fig. 1 shows a dotted line around relevant components labeled "Processor" there is nothing in applicants' original disclosure to limit such components to the same computer chip or the same computer board, or same external housing, or same rack, or same room, etc.

The drawing provides no definition for the term integrated other than to say they work with one another in terms of hardware and software as do Chase's relevant components (see parent application 09/418,520).

27. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: For Figure 2, many of the elements described as being elements of Figure 2 on pages 8 and 9 of the specification are, apparently, absent from the figure or mislabeled. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

28. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: In Fig. 2 there is a box labeled 20 which is not described as an element of Fig. 2 in the detailed description of Figure 2 on pages 8 and 9 of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37

CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

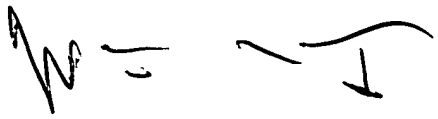
29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

30. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

31. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175. The examiner works at home on Wednesdays but may normally be reached on Wednesdays by leaving a voice message using his office phone number. The examiner also works a flexible schedule but may

normally be reached in the afternoon and evening on three of the four remaining weekdays.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



WILLIAM M. TREAT
PRIMARY EXAMINER